APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/737,262	12/13/2000	Karsten Laubner	P00,1942	1922

7590	03/22/2004

KEVIN R. SPIVAK
MORRRISON & FOERSTER LLP
2000 PENNSYLVANIA AVENUE, N.W.
WASHINGTON, DC 20006-1888

EXAMINER
SEFCHECK, GREGORY B

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date *5, 8*.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2.   Claims 1-3, 6-9, 11-13, 16, 17, and 19 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Jonsson (US 4,809,259).

-     In regards to Claims 1, 3, 11, and 19,

Jonsson discloses a method and device for maintaining synchronization of time

slots in a switching network (Abstract; claim 1/11 – monitoring a correct time slot

sequence in a time/space switching network for a time or space allocation of data

channels to be switched).

Jonsson discloses the use of a marking device for inserting markings in a

plurality of successive frames in the time slots of the connection channels to be

switched (Col. 2, lines 1-5). Referring to Fig. 1, Jonsson shows that the value of the

inserted marking is incremented or decremented by a value of 1 (claim 1/11 – inserting

a monitoring value into a predetermined data channel of successive frames to be

switched, wherein the value for each frame is incremented or decremented by a

predetermined value; claim 3/19 – predetermined value = 1 and is derived from a

counter).

Jonsson shows a scanning device at the output of the switching for equalizing

the switching delay of the marked frames by comparing the markings of received data

(Col. 2, lines 12-18).

Jonsson does not explicitly show forming a difference of the inserted contents of

the data channel of successive frames, wherein the difference is equal to the

predetermined value for indicating correct time slot sequence. Jonsson further does not

show outputting an error when the difference does not equal the predetermined value.

Jonsson discloses feeding sequence instructions to a memory included in an

equalizing means for synchronizing the time slots of switched data in response to a

comparison of the markings in successive frames of switched data. A variety of

comparison operations, such as a subtraction of successive frame markings, would

enable a determination as to whether the data time slot sequence is correct (Col. 2,

lines 31- 43; claim 1/11 – forming a difference of data contents of the predetermined

data channel for immediately successive frames, wherein the difference is equal to the

predetermined value for correct time slot sequence or an error is outputted).

It would have been an obvious design choice to one of ordinary skill in the art at

the time of the invention to adapt the comparison step for checking time slot sequence

integrity in the method and device of Jonsson by forming a difference of the inserted

markings of successive frames. Such a comparison operation would enable

determining if the time slots of data have been switched in the proper sequence. The

result of such comparison also enables equalization of sequencing error through

artificial delays.

- In regards to Claims 6 and 16,

Jonsson discloses a method and device for maintaining synchronization of time

slots in a switching network that covers all limitations of the parent claims.

Referring to Fig. 3, Jonsson discloses a plurality of registers R1-R3 for inserting a

plurality of individual markings for input line L (Col. 4, lines 7-43; claim 6/16 – inserting

comprises a plurality of insertion units allocated to an input switching network line).

- In regards to Claims 7 and 17,

Jonsson discloses a method and device for maintaining synchronization of time

slots in a switching network that covers all limitations of the parent claims.

Jonsson shows that the delay detection unit comprises a plurality of Parts

allocated to two or more output lines for equalizing the delay of the data channels and

regaining time slot synchronization (Fig. 4; Col. 2, lines 12-43; claim 7/17 – difference

forming comprises a plurality of difference forming units allocated to two output

switching network lines).

-   In regards to Claims 2, 8, and 12,

Jonsson discloses a method and device for maintaining synchronization of time slots in a switching network that covers all limitations of the parent claims.

Jonsson does not expressly show an error counter allocated to each difference forming unit for counting errors between the comparison of difference and predetermined value.

Referring to Fig. 4, Jonsson discloses a plurality of AND gates allocated for each comparison unit that are utilized for representing the count of error delays with respect to each data channel (Col. 5-6, lines 18-10; claim 2/12 – counting errors for a lack of agreement between the formed difference and predetermined value; claim 8 – error counter comprises a plurality of error counting units allocated to a difference forming unit).

It would have been an obvious design choice to one of ordinary skill in the art at the time of the invention to utilize an arrangement of logic AND gates in the device of Jonsson for counting the delay errors in transmitted data channels. This would enable the counting of errors as well as providing the appropriate delays for equalizing the data and regaining synchronization amongst the various data channels.

- In regards to Claim 9,

Jonsson discloses a method and device for maintaining synchronization of time slots in a switching network that covers all limitations of the parent claims.

Jonsson shows that the inserting means may function along with an equalizing means for producing synchronous frames from non-synchronous frames having multiple delays (Col. 2, lines 31-43; claim 9 – insertion mechanism is fashioned in an equalizer for producing a plurality of synchronous frames from non-synchronous frames).

- In regards to Claim 13,

Jonsson discloses a method and device for maintaining synchronization of time slots in a switching network that covers all limitations of the parent claims.

Referring to Fig. 3, Jonsson shows that the number of individual inserted markings incremented in successive frames is derived from a counter CNT (Col. 4, lines 30-36; claim 13 – monitoring value is incremented by a predetermined value derived from a counter).

3.   Claims 4, 5, 10, 14, 15, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jonsson in view of Cloutier (US 5,790,543).

-     In regards to Claims 4 and 14,

Jonsson discloses a method and device for maintaining synchronization of time slots in a switching network that covers all limitations of the parent claims.

Jonsson does not expressly show identifying time slot sequence integrity by comparing a predetermined value and a subtraction result determined from delayed and undelayed data content.

Cloutier discloses an apparatus and method for correcting jitter in data packets. Cloutier discloses determining a subtraction result from successive (undelayed and once-delayed) PCR values and comparing the result with a predetermined value to correct synchronization of received data (Col. 10, lines 6-67; claim 4/14 – difference forming comprises a delay for delaying a predetermined data channel by one frame; claim 4/14 – determining a subtraction result from the content of a delayed channel and an undelayed channel; claim 4/14 – comparing the result with the predetermined value).

It would have been obvious to one of ordinary skill in the art at the time of the invention to derive the comparison step for checking time slot sequence integrity in the method and device of Jonsson by subtracting successive values of inserted reference data and comparing the result to a predetermined value. This modification is one explicit way of providing the comparison data that forms the basis for the instructions fed to the memory of the equalizing means, thereby enabling validation/correction of the data's time slot sequence.

-     In regards to Claims 5 and 15,

Jonsson v. Cloutier discloses a method and device for maintaining

synchronization of time slots in a switching network that covers all limitations of the

parent claims.

Jonsson discloses a delay for analyzing delayed channels that includes a

memory (Col. 4, lines 47-53; claim 5/15 – delay comprises at least one speech memory

of time/space switching network).

-     In regards to Claims 10 and 18,

Jonsson discloses a method and device for maintaining synchronization of time

slots in a switching network that covers all limitations of the parent claims.

Jonsson does not explicitly show the inserting of marking values in a data

channel to be in a test channel.

Cloutier discloses an apparatus and method for correcting jitter in data packets,

in part by inserting PCR values in an optional adaption field (test channel; claim 10/18 –

inserting a monitoring value in predetermined data channel is in a test channel).

It would have been obvious to one of ordinary skill in the art at the time of the

invention to modify the method and device of Jonsson by inserting marking values in a

test channel of the data packets. This modification would provide a dedicated channel

for the inserted marking used for monitoring time slot sequence integrity that is clearly

partitioned from the data payload.

Conclusion

4.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

- Bohm et al. (US006430180B1) discloses a method and apparatus for switching

  data between bitstreams of a time division multiplexed network

- Jain (US006259677B1) discloses clock synchronization and dynamic jitter

  management for voice over IP and real-time data

- Karlsson (US006215773B1) discloses a method to control a switching unit and

  an arrangement working according to the method

- Lindberg et al. (US006157639A) discloses time switch stages and switches

- Pirinen (US005648962A) discloses a base station in a cellular radio system and

  a cellular radio system

- Murakami et al. (US005113395A) discloses a frame phase aligning system using

  a buffer memory with a reduced capacity

- Renner (US 4,740,961) discloses a frame checking arrangement for duplex time

  multiplexed reframing circuitry

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Gregory B Sefcheck whose telephone number is 703-

305-0633. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Hassan Kizou can be reached on 703-305-4744. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

GBS
3-15-2004

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600